

Diamond Computer Systems

N Noddings

Quantum Information Processing with Diamond Steven
Prawer,Igor Aharonovich,2014-05-12 Diamond nitrogen vacancy (NV) color centers can transform quantum information science into practical quantum information technology, including fast, safe computing. Quantum Information Processing with Diamond looks at the principles of quantum information science, diamond materials, and their applications. Part one provides an introduction to quantum information processing using diamond, as well as its principles and fabrication techniques. Part two outlines experimental demonstrations of quantum information processing using diamond, and the emerging applications of diamond for quantum information science. It contains chapters on quantum key distribution, quantum microscopy, the hybridization of quantum systems, and building quantum optical devices. Part three outlines promising directions and future trends in diamond technologies for quantum information processing and sensing. Quantum Information Processing with Diamond is a key reference for R&D managers in industrial sectors such as conventional electronics, communication engineering, computer science, biotechnology, quantum optics, quantum mechanics, quantum computing, quantum cryptology, and nanotechnology, as well as academics in physics, chemistry, biology, and engineering. Brings together the topics of diamond and quantum information processing Looks at applications such as quantum computing, neural circuits, and in vivo monitoring of processes at the molecular scale

Designing SOC's with Configured Cores Steve
Leibson,2006-08-15 Microprocessor cores used for SOC design are the direct descendents of Intel's original 4004 microprocessor. Just as packaged microprocessor ICs vary widely in their attributes, so do microprocessors packaged as IP cores. However, SOC designers still compare and select processor cores the way they previously compared and selected packaged

microprocessor ICs. The big problem with this selection method is that it assumes that the laws of the microprocessor universe have remained unchanged for decades. This assumption is no longer valid. Processor cores for SOC designs can be far more plastic than microprocessor ICs for board-level system designs. Shaping these cores for specific applications produces much better processor efficiency and much lower system clock rates. Together, Tensilica's Xtensa and Diamond processor cores constitute a family of software-compatible microprocessors covering an extremely wide performance range from simple control processors, to DSPs, to 3-way superscalar processors. Yet all of these processors use the same software-development tools so that programmers familiar with one processor in the family can easily switch to another. This book emphasizes a processor-centric MPSOC (multiple-processor SOC) design style shaped by the realities of the 21st-century and nanometer silicon. It advocates the assignment of tasks to firmware-controlled processors whenever possible to maximize SOC flexibility, cut power dissipation, reduce the size and number of hand-built logic blocks, shrink the associated verification effort, and minimize the overall design risk. · An essential, no-nonsense guide to the design of 21st-century mega-gate SOC designs using nanometer silicon. · Discusses today's key issues affecting SOC design, based on author's decades of personal experience in developing large digital systems as a design engineer while working at Hewlett-Packard's Desktop Computer Division and at EDA workstation pioneer Cadnetix, and covering such topics as an award-winning technology journalist and editor-in-chief for EDN magazine and the Microprocessor Report. · Explores conventionally accepted boundaries and perceived limits of processor-based system design and then explodes these artificial constraints through a fresh outlook on and discussion of the special abilities of processor cores designed specifically for SOC design. · Thorough exploration of the evolution of processors and processor cores

used for ASIC and SOC design with a look at where the industry has come from, and where it's going. · Easy-to-understand explanations of the capabilities of configurable and extensible processor cores through a detailed examination of Tensilica's configurable, extensible Xtensa processor core and six pre-configured Diamond cores. · The most comprehensive assessment available of the practical aspects of configuring and using multiple processor cores to achieve very difficult and ambitious SOC price, performance, and power design goals.

Diamond High Assurance Security Program: Trusted Computing Exemplar ,2002 Over the past decade, the U.S. Government has not been significantly involved in high assurance Trusted Computing acquisitions and research. During this time, the Government's focus on commercial off the shelf procurements helped to fuel explosive advances in commercial technology, but it also contributed to the lack of progress in the ability of commercial systems to appropriately protect themselves and the data with which they are entrusted. While industry has been driven to supply the latest technology at the fastest pace, it has not been motivated, either internally or externally via customer demand, to produce highly trustworthy computing systems. As a result, the National Information Infrastructure is weak; there are no high security, high assurance, off-the-shelf products available that can be used to strengthen it; and the National capability to design and construct such trusted computer systems and networks has atrophied. To address this downward spiral, the Center for INFOSEC Studies and Research (CISR) in Monterey, California, proposes a Trusted Computing Exemplar project that will provide an openly distributed worked example of how high assurance trusted computing components can be built. Completion of this project will be performed as part of CISR's Diamond High Assurance Security Program (Diamond HASP). The authors propose four related activities: (1) creation of a prototype framework for rapid high assurance system development, (2)

development of a reference-implementation trusted computing component, (3) evaluation of the component for high assurance, and (4) open dissemination of deliverables related to the first three activities. The project's open development methodology will provide widespread availability of key high assurance enabling technologies and ensure transfer of knowledge and capabilities for trusted computing to the next generation of developers, evaluators, and educators. (1 figure, 9 refs.).

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High-Performance Computing Systems and Technologies in Scientific Research, Automation of Control and Production Vladimir Jordan,Ilya Tarasov,Vladimir Faerman,2022-01-17 This book constitutes selected revised and extended papers from the 11th International Conference on High-Performance Computing Systems and Technologies in Scientific Research, Automation of Control and Production, HPCST 2021, Barnaul, Russia, in May 2021. The 32 full papers presented in this volume were thoroughly reviewed and selected from 98 submissions. The papers are organized in topical sections on Hardware for High-Performance Computing and Signal

Processing; Information Technologies and Computer Simulation of Physical Phenomena; Computing Technologies in Discrete Mathematics and Decision Making; Information and Computing Technologies in Automation and Control Science; and Computing Technologies in Information Security Applications.

Diamond HASP Trusted Computing Exemplar ,2002 The National Information Infrastructure is weak; there are no high security, high assurance, off-the-shelf products available that can be used to strengthen it; and the National capability to design and construct such trusted computer systems and networks has atrophied. The purpose of the Trusted Computing Exemplar project is to provide a worked example to show how trusted computing systems and components can be constructed. A prototype high assurance development framework will be created first, and then used to produce a reference implementation trusted computing component the Embedded MicroKernel Prototype. A third-party evaluation of the component will be initiated during development (e.g., once the high-level design documentation is written). The documentation, source code, development framework and other deliverables will be made openly available as they are produced. We will develop a high assurance, embedded micro-kernel and a trusted application built on top of the micro-kernel as a reference implementation exemplar for trusted computing. Because the product as well as the process will be showpieces for trusted computing development, high assurance methodologies and techniques will be applied during the entire lifecycle. The goal is to produce a very small, portable component that will provide users with correct security operation and an a priori assurance against system subversion.

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Embedded Computer Systems: Architectures, Modeling, and Simulation Cristina Silvano,Christian Pilato,Marc Reichenbach,2023-12-08 This book constitutes the proceedings of the 22st International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, SAMOS 2021, which took place in July 2022 in Samos, Greece. The 11 full papers and 7 short papers presented in this volume were carefully reviewed and selected from 45 submissions. The

conference covers a wide range of embedded systems design aspects, including machine learning accelerators, and power management and programmable dataflow systems.

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InfoWorld ,1994-04-04 InfoWorld is targeted to Senior IT professionals. Content is segmented into Channels and Topic Centers. InfoWorld also celebrates people, companies, and projects.

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Introduction to Computer Systems Harold L. Rogler,2013-03-07

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