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Vassil Dimitrov,Graham Jullien,Roberto Muscedere

Digital Design from Zero to One Jerry D. Daniels, 1996-04-19 Takes a fresh look at basic digital design. From definition, to example, to graphic illustration, to simulation result, the book progresses through the main themes of digital design. Technically up-to-date, this book covers all the latest topics: Field programmable gate arrays, PALs and ROMs. The latest memory chips for SRAM and DRAM are shown. Software for creating the excitation equations of FSM are covered, as well as LogicWorks and Beige Bag PC and more.

Multiple-Base Number System Vassil Dimitrov, Graham Jullien, Roberto Muscedere, 2017-12-19 Computer arithmetic has become so fundamentally embedded into digital design that many engineers are unaware of the many research advances in the area. As a result, they are losing out on emerging opportunities to optimize its use in targeted applications and technologies. In many cases, easily available standard arithmetic hardware might not necessarily be the most efficient implementation strategy. Multiple-Base Number System: Theory and Applications stands apart from the usual books on computer arithmetic with its concentration on the uses and the mathematical operations associated with the recently introduced multiple-base number system (MBNS). The book identifies and explores several diverse and never-before-considered MBNS applications (and their implementation issues) to enhance computation efficiency, specifically in digital signal processing (DSP) and public key cryptography. Despite the recent development and increasing popularity of MBNS as a specialized tool for high-performance calculations in electronic hardware and other fields, no single text has compiled all the crucial, cutting-edge information engineers need to optimize its use. The authors' main goal was to disseminate the results of extensive design research—including much of their own—to help the widest possible audience of engineers, computer scientists, and mathematicians. Dedicated to helping readers apply discoveries in advanced integrated circuit technologies, this single reference is packed with a wealth of vital content previously scattered throughout limited-circulation technical and mathematical journals and papers—resources generally accessible only to researchers and designers working in highly specialized fields. Leveling the informational playing field, this resource guides readers through an in-depth analysis of theory, architectural techniques, and the latest research on the subject, subsequently laying the groundwork users require to begin applying MBNS.

Residue Number Systems P.V. Ananda Mohan, 2012-12-06 There has been continuing interest in the improvement of the speed of Digital Signal processing. The use of Residue Number Systems for the design of DSP systems has been extensively researched in literature. Szabo and Tanaka have popularized this approach through their book published in 1967. Subsequently, Jenkins and Leon have rekindled the interest of researchers in this area in 1978, from which time there have been several efforts to use RNS in practical system implementation. An IEEE Press book has been published in 1986 which was a collection of Papers. It is very interesting to note that in the recent past since 1988, the research activity has received a new thrust with emphasis on VLSI design using non ROM based designs as well as ROM based designs as evidenced by the increased publications in this area. The main advantage in using RNS is that several small word-length Processors are used to perform operations such as addition, multiplication and accumulation, subtraction, thus needing less instruction execution time than that needed in conventional 16 bit/32 bit DSPs. However, the disadvantages of RNS have been the difficulty of detection of overflow, sign detection, comparison of two numbers, scaling, and division by arbitrary number, RNS to Binary conversion and Binary to RNS conversion. These operations, unfortunately, are computationally intensive and are time consuming.

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Computer Arithmetic Behrooz Parhami, 2010 Ideal for graduate and senior undergraduate courses in computer arithmetic and advanced digital design, Computer Arithmetic: Algorithms and Hardware Designs, Second Edition, provides a balanced, comprehensive treatment of computer arithmetic. It covers topics in arithmetic unit design and circuit implementation that complement the architectural and algorithmic speedup techniques used in high-performance computer architecture and parallel processing. Using a unified and consistent framework, the text begins with number representation and proceeds through basic arithmetic operations, floating-point arithmetic, and function evaluation methods. Later chapters cover broad design and implementation topics—including techniques for high-throughput, low-power, fault-tolerant, and reconfigurable arithmetic. An appendix provides a historical view of the field and speculates on its future. An indispensable resource for instruction, professional development, and research, Computer Arithmetic: Algorithms and Hardware Designs, Second Edition, combines broad coverage of the underlying theories of computer arithmetic with numerous examples of practical designs, worked-out examples, and a large collection of meaningful problems. This second edition includes a new chapter on reconfigurable arithmetic, in order to address the fact that arithmetic functions are increasingly being implemented on field-programmable gate arrays (FPGAs) and FPGA-like configurable devices. Updated and thoroughly revised, the book offers new and expanded coverage of saturating adders and multipliers, truncated multipliers, fused multiply-add units, overlapped quotient digit selection, bipartite and multipartite tables, reversible logic, dot notation, modular arithmetic, Montgomery modular reduction, division by constants, IEEE floating-point standard formats, and interval arithmetic.

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DSP system is to identify for each of its components an implementation architecture that provides the desired degree of flexibility/programmability and optimises the area-delay-power parameters. This essential book covers architectures that offer varying degrees of programmability.

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Official Gazette of the United States Patent Office United States. Patent Office, 1969

Official Gazette of the United States Patent and Trademark Office ,1999

Process Control ,

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Computers & Electronics ,1984

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