Xilinx Pocket Power Estimator

Michal Rosen-Zvi

Architecture of Computing Systems -- ARCS 2013 Hana Kubatova, Christian Hochberger, Martin Dan k, Bernhard Sick, 2013-02-12 This book constitutes the refereed proceedings of the 26th International Conference on Architecture of Computing Systems, ARCS 2013, held in Prague, Czech Republic, in February 2013. The 29 papers presented were carefully reviewed and selected from 73 submissions. The topics covered are computer architecture topics such as multi-cores, memory systems, and parallel computing, adaptive system architectures such as reconfigurable systems in hardware and software, customization and application specific accelerators in heterogeneous architectures, organic and autonomic computing including both theoretical and practical results on self-organization, self-configuration, self-optimization, self-healing, and self-protection techniques, operating systems including but not limited to scheduling, memory management, power management, RTOS, energy-awareness, and green computing.

Low Power Design with High-Level Power Estimation and Power-Aware Synthesis Sumit

Ahuja, Avinash Lakshminarayana, Sandeep Kumar Shukla, 2011-10-22 This book presents novel
research techniques, algorithms, methodologies and experimental results for high level power
estimation and power aware high-level synthesis. Readers will learn to apply such techniques to
enable design flows resulting in shorter time to market and successful low power ASIC/FPGA design.

Power Estimation on Electronic System Level using Linear Power Models Stefan

Schuermans,Rainer Leupers,2018-12-14 This book describes a flexible and largely automated methodology for adding the estimation of power consumption to high level simulations at the electronic system level (ESL). This method enables the inclusion of power consumption considerations from the very start of a design. This ability can help designers of electronic systems to create devices with low power consumption. The authors also demonstrate the implementation of the method, using the popular ESL language "SystemC". This implementation enables most existing SystemC ESL simulations for power estimation with very little manual work. Extensive case-studies of a Network on Chip communication architecture and a dual-core application processor "ARM Cortex-A9" showcase the applicability and accuracy of the method to different types of electronic devices. The evaluation compares various trade-offs regarding amount of manual work, types of ESL models, achieved estimation accuracy and impact on the simulation speed. Describes a flexible and largely automated ESL power estimation method; Shows implementation of power estimation methodology in SystemC; Uses two extensive case studies to demonstrate method introduced.

Low Power Design with High-Level Power Estimation and Power-Aware Synthesis, 2011-10-22 Power Analyzer for Pocket Computing (PAPC). ,2004 Under this contract researchers at the Universities of Michigan and Colorado have developed an innovative and practical power evaluation tool, Power Analyzer, suitable for calculating power consumption for complete computer systems. Power Analyzer will be initially targeted to pocket computers where computing and communication place strong demands on the portable power supply.

Transaction–Level Power Modeling Amr Baher Darwish, Magdy Ali El-Moursy, Mohamed Amin Dessouky, 2020-08-25 This book describes for readers a methodology for dynamic power estimation, using Transaction Level Modeling (TLM). The methodology exploits the existing tools for RTL simulation, design synthesis and SystemC prototyping to provide fast and accurate power estimation using Transaction Level Power Modeling (TLPM). Readers will benefit from this innovative way of evaluating power on a high level of abstraction, at an early stage of the product life cycle, decreasing the number of the expensive design iterations.

High-level Synthesis Michael Fingeroff,2010 Are you an RTL or system designer that is currently using, moving, or planning to move to an HLS design environment? Finally, a comprehensive guide for designing hardware using C++ is here. Michael Fingeroff's High-Level Synthesis Blue Book presents the most effective C++ synthesis coding style for achieving high quality RTL. Master a totally new design methodology for coding increasingly complex designs! This book provides a step-by-step approach to using C++ as a hardware design language, including an introduction to the basics of HLS using concepts familiar to RTL designers. Each chapter provides easy-to-understand C++ examples, along with hardware and timing diagrams where appropriate. The book progresses from simple concepts such as sequential logic design to more complicated topics such as memory architecture and hierarchical sub-system design. Later chapters bring together many of the earlier HLS design concepts through their application in simplified design examples. These examples illustrate the fundamental principles behind C++ hardware design, which will translate to much larger designs. Although this book focuses primarily on C and C++ to present the basics of C++ synthesis, all of the concepts are equally applicable to SystemC when describing the core algorithmic part of a design. On completion of this book, readers should be well on their way to becoming experts in high-level synthesis.

Exploring Zynq Mpsoc CROCKETT H. DAVID LOUISE (NORTHCOTE. CRAIG, RAMSAY.),Northcote David,Ramsay Craig,2019-04-11 This book introduces the Zynq MPSoC (Multi-Processor System-on-Chip), an embedded device from Xilinx. The Zynq MPSoC combines a

sophisticated processing system that includes ARM Cortex-A53 applications and ARM Cortex-R5 real-time processors, with FPGA programmable logic. As well as guiding the reader through the architecture of the device, design tools and methods are also covered in detail: both the conventional hardware/software co-design approach, and the newer software-defined methodology using Xilinx's SDx development environment. Featured aspects of Zynq MPSoC design include hardware and software development, multiprocessing, safety, security and platform management, and system booting. There are also special features on PYNQ, the Python-based framework for Zynq devices, and machine learning applications. This book should serve as a useful guide for those working with Zynq MPSoC, and equally as a reference for technical managers wishing to gain familiarity with the device and its associated design methodologies.

21st International Conference on Distributed Computing Systems Workshops Makoto
Takizawa,2001 Annotation Proceedings of an April 2001 set of workshops of applied reliable group
communication, distributed dynamic multiservice architectures, smart appliances and wearable
computing, multimedia network systems, and wireless networks and mobile computing. Specific
subjects covered include the architecture of a secure group communication system based on intrusion
tolerance, client side reconfiguration on software components for load balancing, collaborative media
streaming in an in- home network, experimental evaluation of error control for video multicast over
wireless LANs, image indexing and similarity retrieval based on a new spatial relation model, and a
multi-channel MAC protocol with power control for multi-hop mobile ad hoc networks. Lacks a subject
index. c. Book News Inc.

Software-Defined Radio for Engineers Alexander M. Wyglinski,Robin Getz,Travis Collins,Di
Pu,2018-04-30 Based on the popular Artech House classic, Digital Communication Systems
Engineering with Software-Defined Radio, this book provides a practical approach to quickly learning
the software-defined radio (SDR) concepts needed for work in the field. This up-to-date volume guides
readers on how to quickly prototype wireless designs using SDR for real-world testing and
experimentation. This book explores advanced wireless communication techniques such as OFDM,
LTE, WLA, and hardware targeting. Readers will gain an understanding of the core concepts behind
wireless hardware, such as the radio frequency front-end, analog-to-digital and digital-to-analog
converters, as well as various processing technologies. Moreover, this volume includes chapters on
timing estimation, matched filtering, frame synchronization message decoding, and source coding. The
orthogonal frequency division multiplexing is explained and details about HDL code generation and

deployment are provided. The book concludes with coverage of the WLAN toolbox with OFDM beacon reception and the LTE toolbox with downlink reception. Multiple case studies are provided throughout the book. Both MATLAB and Simulink source code are included to assist readers with their projects in the field.

Designing with Xilinx® FPGAs Sanjay Churiwala,2016-10-20 This book helps readers to implement their designs on Xilinx® FPGAs. The authors demonstrate how to get the greatest impact from using the Vivado® Design Suite, which delivers a SoC-strength, IP-centric and system-centric, next generation development environment that has been built from the ground up to address the productivity bottlenecks in system-level integration and implementation. This book is a hands-on guide for both users who are new to FPGA designs, as well as those currently using the legacy Xilinx tool set (ISE) but are now moving to Vivado. Throughout the presentation, the authors focus on key concepts, major mechanisms for design entry, and methods to realize the most efficient implementation of the target design, with the least number of iterations.

Independent Component Analyses, Wavelets, Unsupervised Nano-biomimetic Sensors, and Neural Networks V Harold H. Szu, Jack Agee, 2007 Proceedings of SPIE present the original research papers presented at SPIE conferences and other high-quality conferences in the broad-ranging fields of optics and photonics. These books provide prompt access to the latest innovations in research and technology in their respective fields. Proceedings of SPIE are among the most cited references in patent literature.

Verilog® Quickstart James M. Lee,2006-04-18 From a review of the Second Edition 'If you are new to the field and want to know what all this Verilog stuff is about, you've found the golden goose. The text here is straight forward, complete, and example rich -mega-multi-kudos to the author James Lee. Though not as detailed as the Verilog reference guides from Cadence, it likewise doesn't suffer from the excessive abstractness those make you wade through. This is a quick and easy read, and will serve as a desktop reference for as long as Verilog lives. Best testimonial: I'm buying my fourth and fifth copies tonight (I've loaned out/lost two of my others).' Zach Coombes, AMD

STRUCTURED COMPUTER ORGANIZATION, 1996

Fabless Daniel Nenni, Paul Michael McLellan, 2014 The purpose of this book is to illustrate the magnificence of the fabless semiconductor ecosystem, and to give credit where credit is due. We trace the history of the semiconductor industry from both a technical and business perspective. We argue that the development of the fabless business model was a key enabler of the growth in

semiconductors since the mid-1980s. Because business models, as much as the technology, are what keep us thrilled with new gadgets year after year, we focus on the evolution of the electronics business. We also invited key players in the industry to contribute chapters. These In Their Own Words chapters allow the heavyweights of the industry to tell their corporate history for themselves, focusing on the industry developments (both in technology and business models) that made them successful, and how they in turn drive the further evolution of the semiconductor industry.

Electrical & Electronics Abstracts ,1997

RTL Hardware Design Using VHDL Pong P. Chu, 2006-04-20 The skills and guidance needed to master RTL hardware design This book teaches readers how to systematically design efficient, portable, and scalable Register Transfer Level (RTL) digitalcircuits using the VHDL hardware description language and synthesissoftware. Focusing on the module-level design, which is composed offunctional units, routing circuit, and storage, the bookillustrates the relationship between the VHDL constructs and theunderlying hardware components, and shows how to develop codes thatfaithfully reflect the module-level design and can be synthesized into efficient gate-level implementation. Several unique features distinguish the book: * Coding style that shows a clear relationship between VHDLconstructs and hardware components * Conceptual diagrams that illustrate the realization of VHDLcodes * Emphasis on the code reuse * Practical examples that demonstrate and reinforce designconcepts, procedures, and techniques * Two chapters on realizing sequential algorithms in hardware * Two chapters on scalable and parameterized designs and coding * One chapter covering the synchronization and interface betweenmultiple clock domains Although the focus of the book is RTL synthesis, it also examines the synthesis task from the perspective of the overall developmentprocess. Readers learn good design practices and guidelines toensure that an RTL design can accommodate future simulation, verification, and testing needs, and can be easily incorporated into a larger system or reused. Discussion is independent oftechnology and can be applied to both ASIC and FPGA devices. With a balanced presentation of fundamentals and practical examples, this is an excellent textbook for upper-levelundergraduate or graduate courses in advanced digital logic. Engineers who need to make effective use of today's synthesissoftware and FPGA devices should also refer to this book.

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Xilinx Pocket Power Estimator Introduction

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